Design Considerations for the DDR3 Memory Sub-system

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1. DDR2 vs. DDR3 Feature Comparison
2. DDR3 DQ Signaling
3. DDR3 CK/Control/Address Net Topology
4. Summary

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1. **DDR2** vs. **DDR3 Feature Comparison**
2. **DDR3 DQ Signaling**
3. **DDR3 CK/Control/Address Net Topology**
4. **Summary**

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DDR3 Feature Comparison

	DDR	DDR2	DDR3[*1]
Data Rate	200 ~ 400 Mbps	400 ~ 800 Mbps	800 ~ 1600 Mbps[*2]
System Assumption	4slots(8loads)	2slot(4loads)	2slot(4loads)[*2]
Vdd/Vddq	2.5V ± 0.2V	1.8V ± 0.1V	1.5V ± 0.075V
Interface	SSTL_2	SSTL_18	SSTL_15
Package	66TSOP2 60 BGA	60 BGA for x4/x8 84 BGA for x16	78 BGA for x4/x8 96 BGA for x16
Source sync.	Bi-directional DQS (Single ended Default)	Bi-directional DQS (Single./Diff. Option)	Bi-directional DQS (Differential Default)
Burst Length	BL=2,4,8 (2bits Prefetch)	BL = 4, 8 (4bits Prefetch)	BL = 4, 8 (8bits Prefetch)
# of bank	4banks	512Mb : 4banks 1Gb : 8banks	512Mb/1Gb: 8 banks 2Gb/4Gb/8Gb: tbd
CL/tRCD/tRP	~15/15/15ns	~ 15/15/15 ns	~ 12/12/12 ns
Reset	No	No	Yes
ODT	No	Yes	Yes
Driver Calibration	No	Off-Chip Driver Calibration	Self calibration with ZQ Pin
Leveling	No	No	Yes

Note 1: DDR3 Key Features have been fixed in JEDEC.

Note 2: Max. Frequency by DDR3 System Assumption is under discussion.
DDR3 supports 1600Mbps under 1slot/channel system.
And, the Possibility of DDR3 2-Slot/channel system being discussed in JEDEC.

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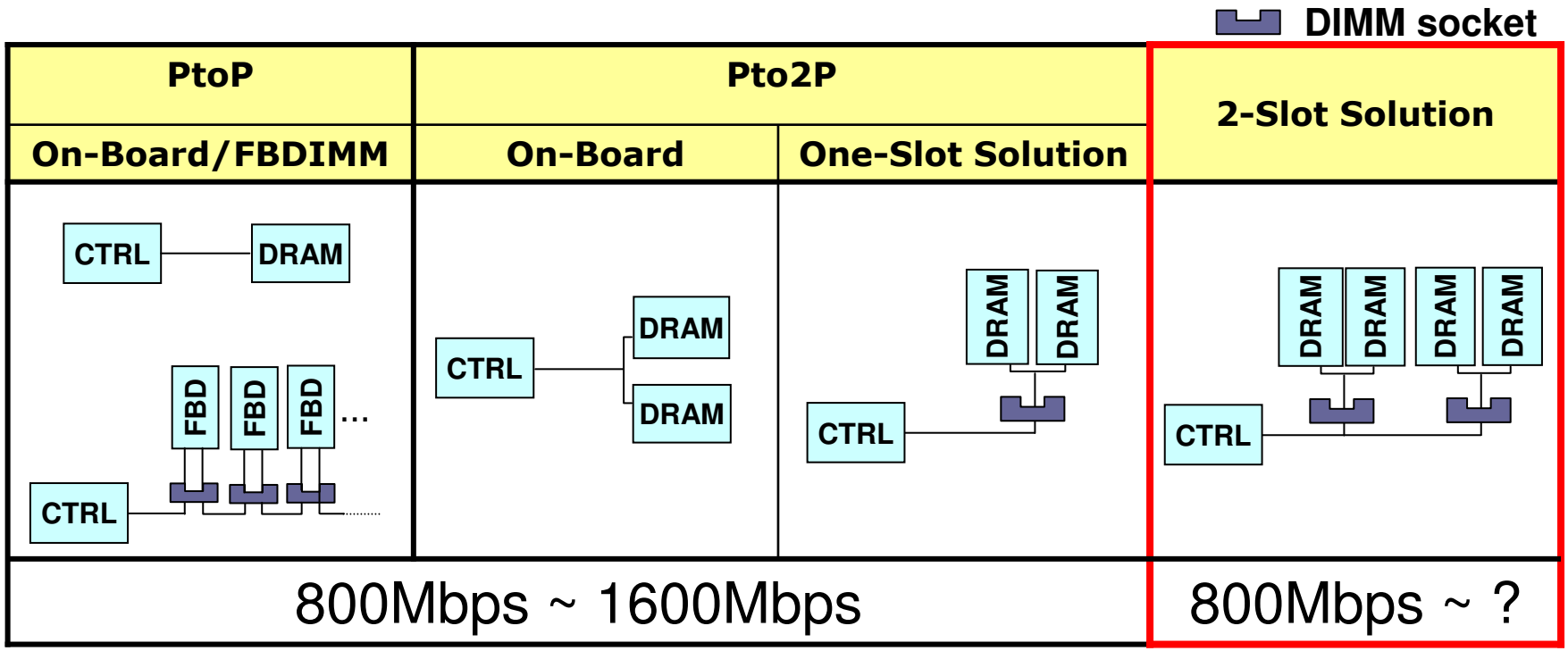
DDR3 System Assumption

- **DDR3: System Assumption & Max. Frequency**



- **Max. Frequency of DDR3 2-Slot/Channel under study at JEDEC**

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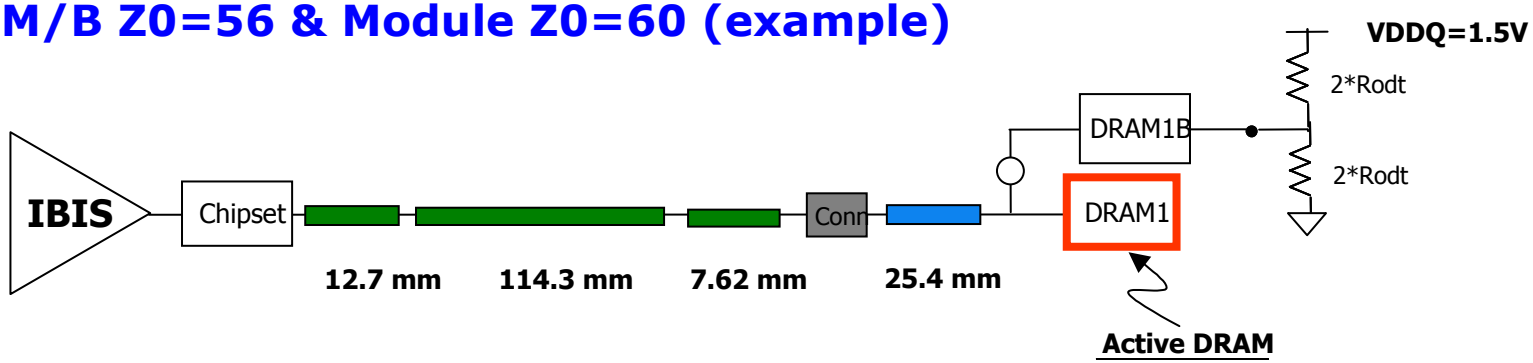
DDR3 DQ channel modeling

❑ M/B Z0=56 & Module Z0=60 (example)



Cf. Slot to Slot Distance(@2slots system) : 10.16mm(0.4inch)

❑ Common Parameters

DRAM Param	Values
Cpkg	0.7 pF
Cdie	Depends on linearity
Cin	Cdie + Cpkg
Lpkg	3.0 nH
Rdie	4.0 ohm

Chipset Param	Values
Cdie	Assume same as DRAM

❑ P22P Channel ODT Control

Operation		MCH ODT	Rank 1 ODT	Rank 2 ODT
Write	Rank 1	X	X	60
	Rank 2	X	60	X
Read	Rank 1	60	X	X
	Rank 2	60	X	X

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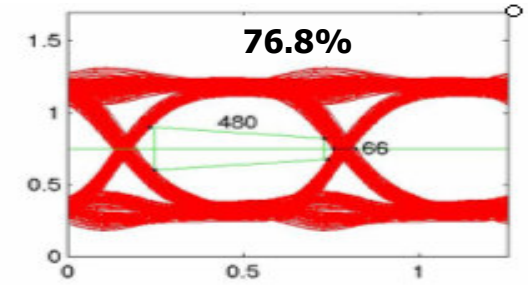
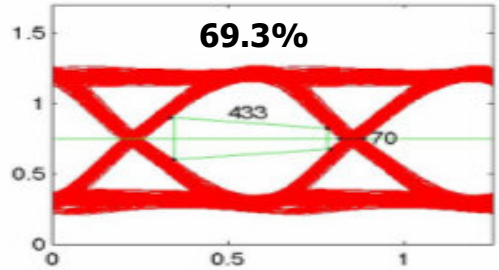
Max. Frequency for DDR3

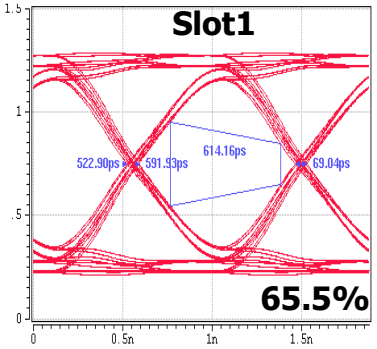
DRAM WRITE | **DRAM READ**

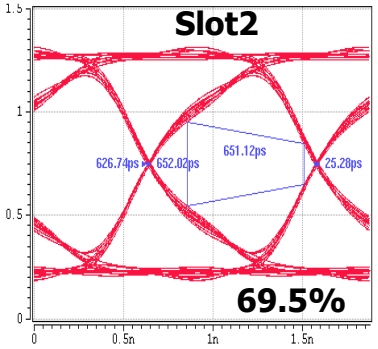
1600Mbps (@1slot system)

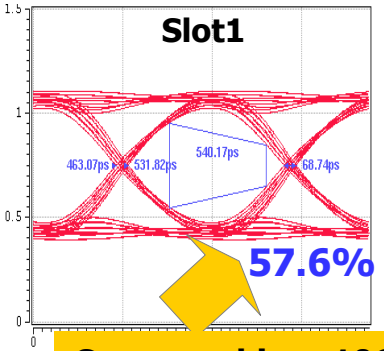


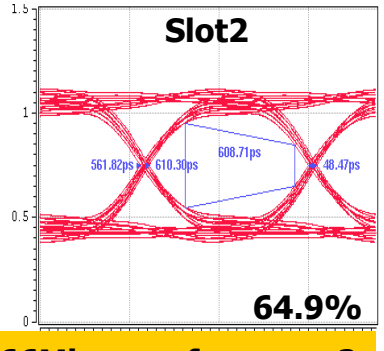


1066Mbps (@2slot system)



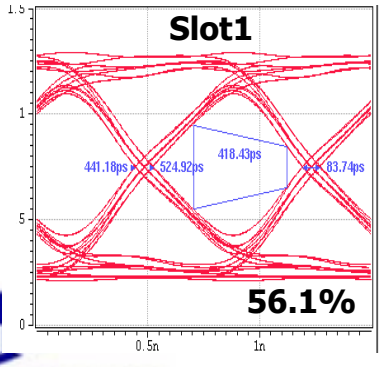


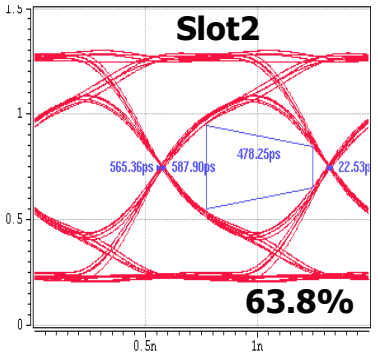


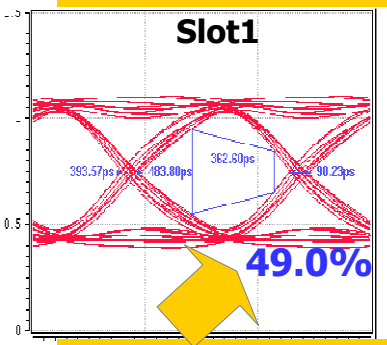


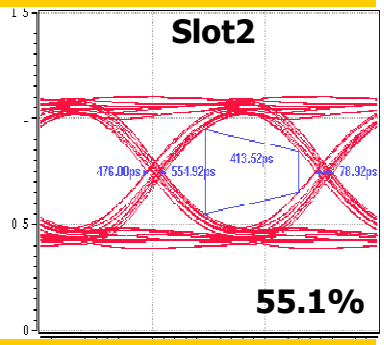
Can we achieve 1066Mbps performance?

1333Mbps (@2slot system)









Can we achieve 1333Mbps performance?

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DQ Design Consideration for DDR3

- For Higher Performance of DQ Channel:
  - **Optimized R_{on} and its linearity**
  - **Optimized ODT and its linearity**
  - **Optimized C_{IO}**
  - **ZQ Calibration (Self-Driver Calibration)**
- More Study Needed for DDR3 2-Slot/Channel Solution
  - **Samsung optimistic about "2-Slots/channel solution at DDR3-1333 with some optimization (Driver/ODT/Channel, etc.)**
  - **1-Slot/Ch does not permit "memory expandability" for users**

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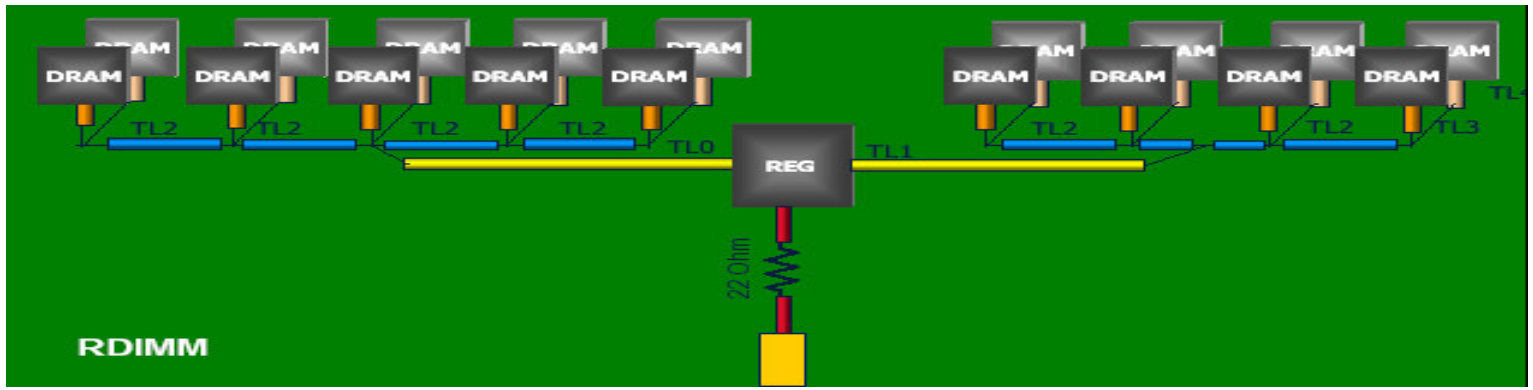
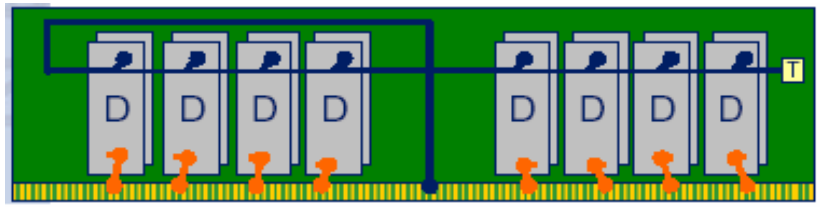
CS/Address/CTRL Net Topology of DIMM

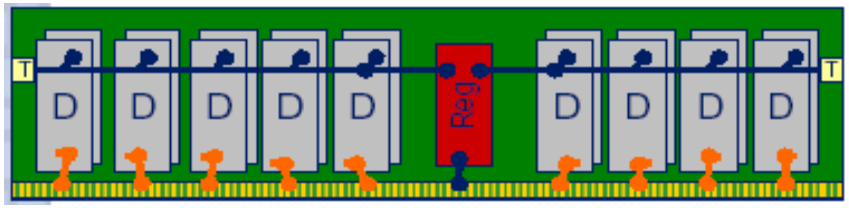
- **As Is (DDR/DDR2): T-branch Topology**



- **With DDR3: Fly-by Topology**
  - **Better signal integrity to reduce # of stubs and stub length**
  - **Easy to apply a single termination at end of signal**



UDIMM



RDIMM

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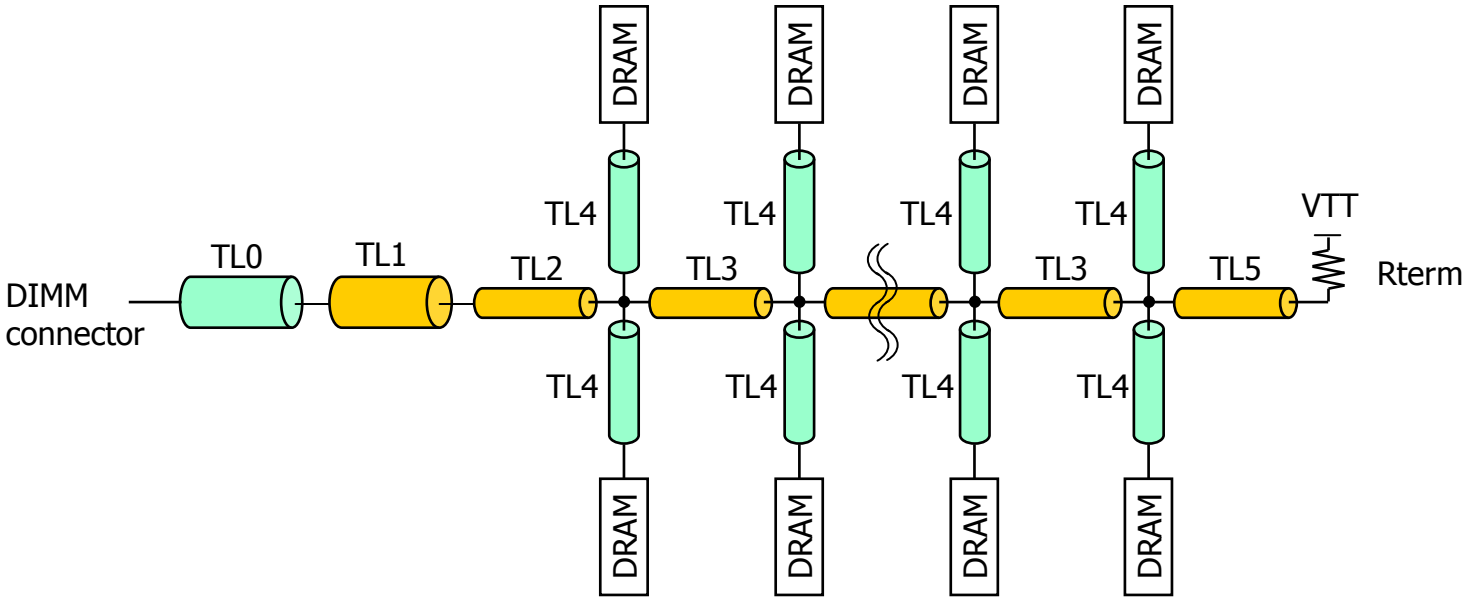
DDR3 CS/CK & CTRL/Add Signal Modeling

❑ CS/CK & CTRL/Address nets (R/C E)

- ➢ **All CS, CK nets have same topology to minimize per-pin skews**



Length [mm]		TL0	TL1	TL0+TL1	TL2	TL3	TL4	TL5
CS / Clock	Min	66.7	9.0	670ps	7.0	14.0	0.6	7.5
	Max	81.0	23.5	671ps	7.05	14. 05	3.0	10.9
CTRL /Address	Min	34.8	78.0	820ps	10.0	14.0	0.6	7.3
	Max	43.0	85.2	821ps	10.05	14. 05	1.5	11.3

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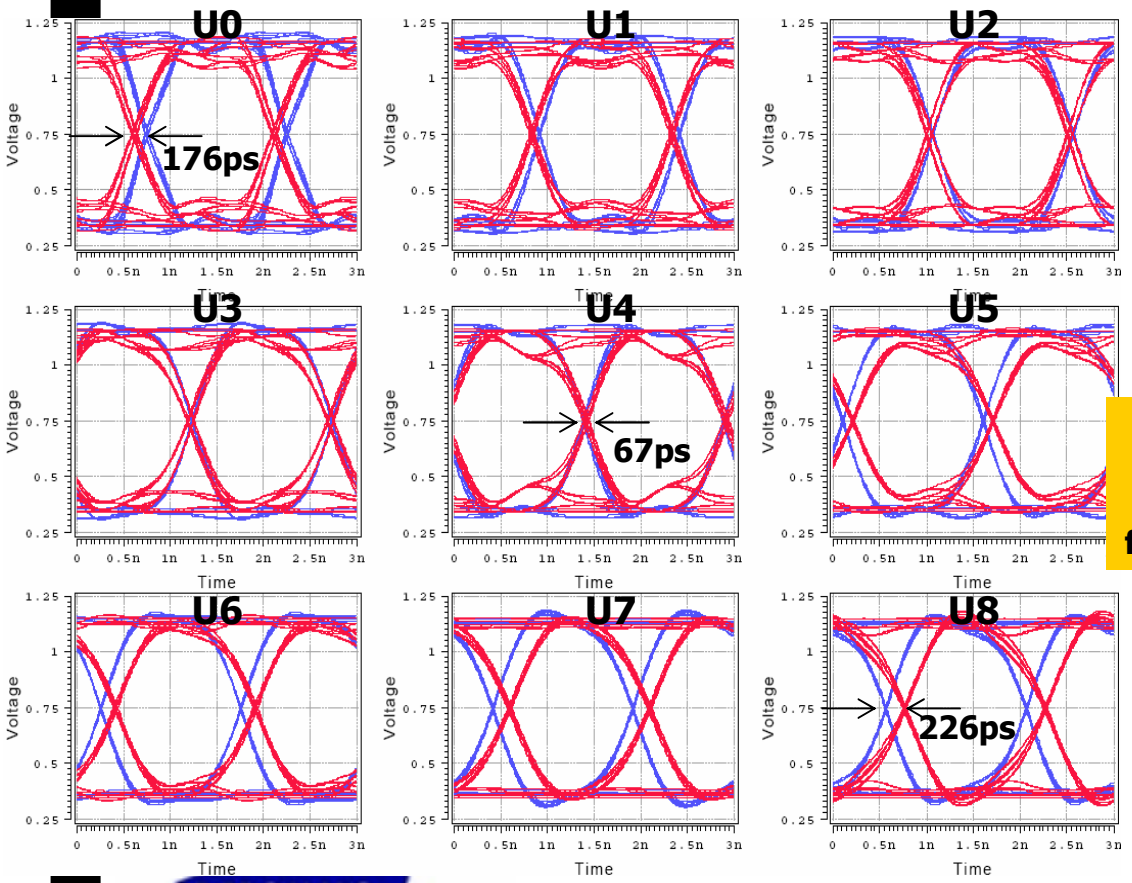
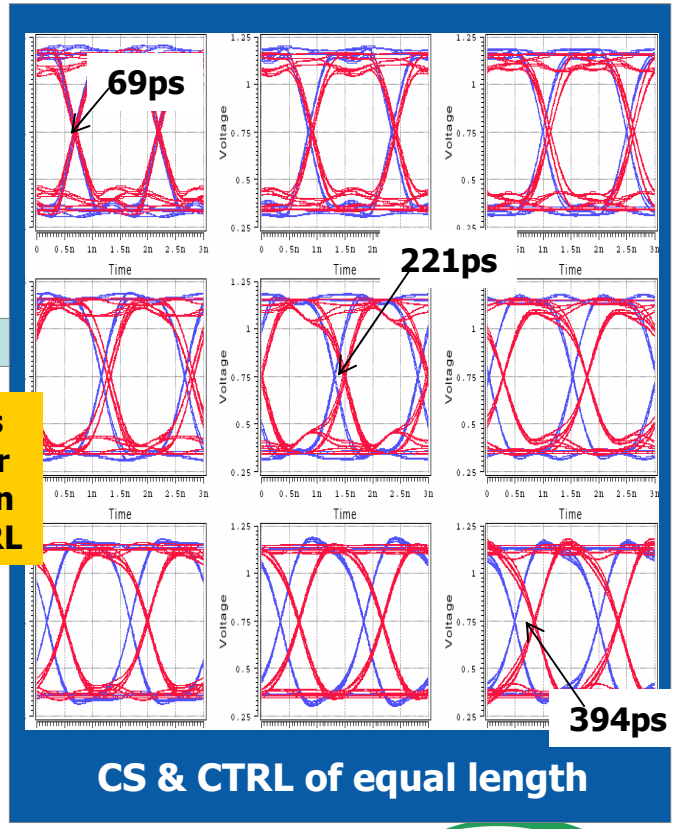
Channel Simulation Results

- **Simulation Results for CS/CK & CRTL/Address (U0~U17)**
  - **Skew between CS/CK and Control/Address**
  - **Longer Control/Address lead-in is helpful**



150ps Longer Lead-in for CTRL



CS & CTRL of equal length

Red Signals : CK/CS Nets , Blue Signal : CRTL/Address Nets

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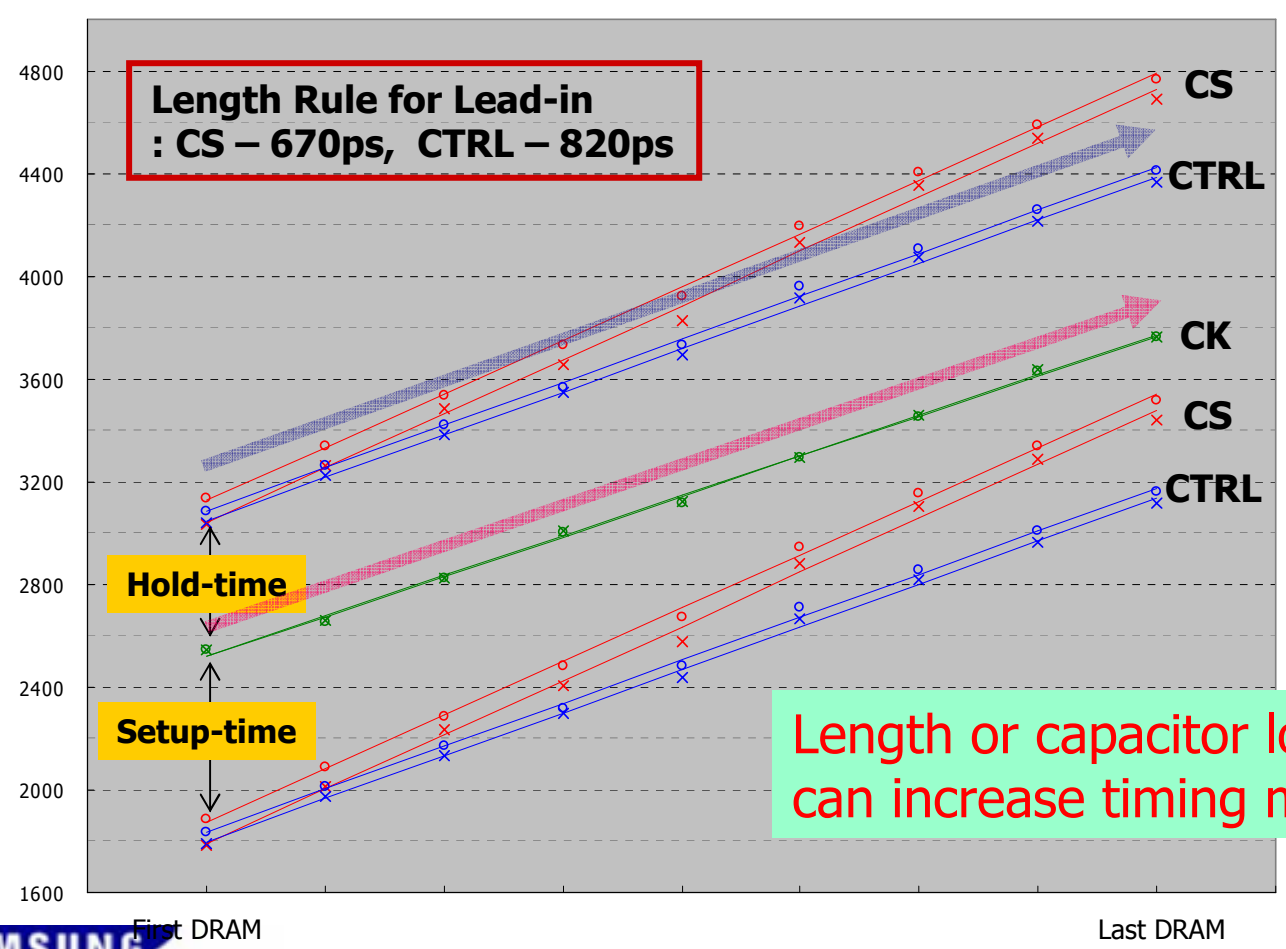
Setup-Hold time under Fly-by Topology

- **tPD : Propagation delay (Driver to Receiver)**



CTRL+150ps

CK+5.1pF

Length or capacitor loading can increase timing margin

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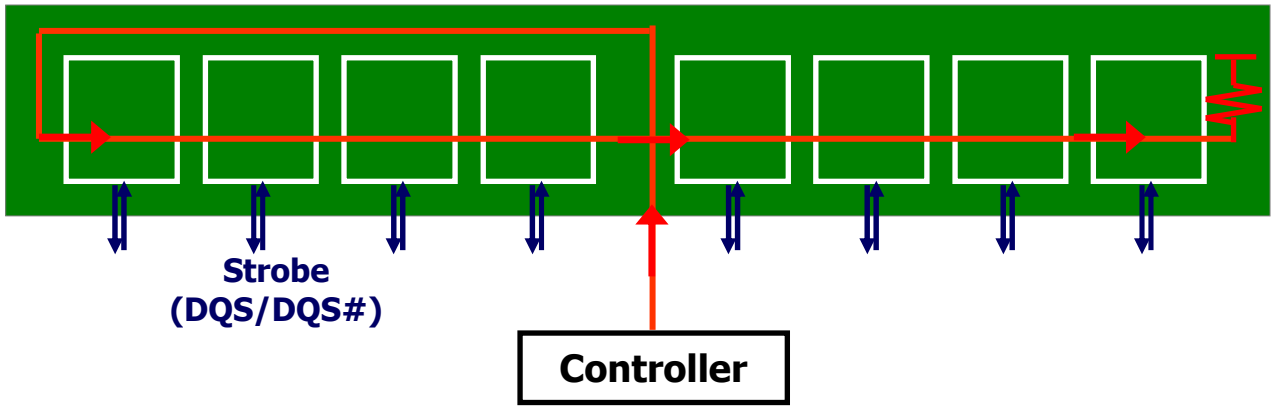
Disadvantage on Fly-by Topology

- **Fly-by Topology Issue in DDR3 Memory Sub System**
  - **Fly-by signals: Command/Address/Control buses & CK**
  - **Flight Time skew between CK and DQS on every DRAM makes tDQSS specification harder to maintain**



- **Controller needs to control "skewing/de-skewing" on each DRAM for DDR3 Memory ("Leveling")**

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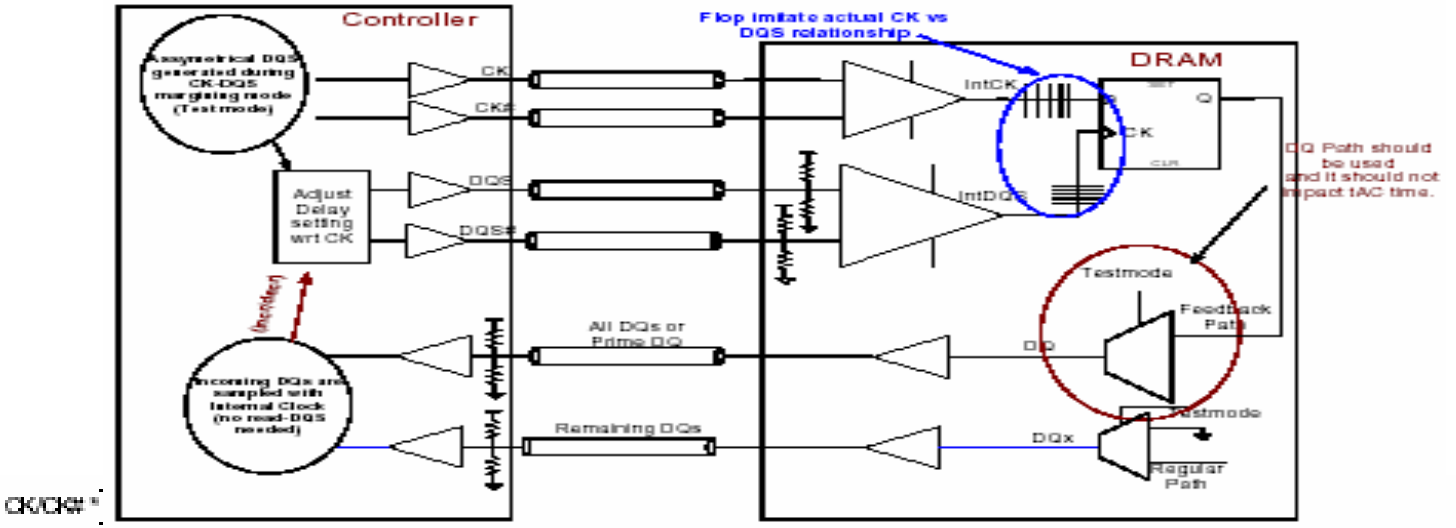
"Leveling"- Write Leveling

Function	EMRS1 Bit	Enable	Disable
Levelization (Margining mode)	7	1	0
Output buffer mode	12	0	1



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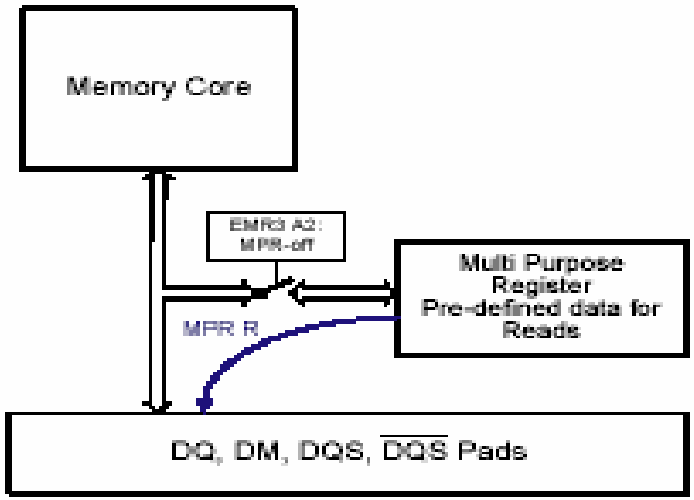
"Leveling"- Read Leveling

❑ Multi Purpose Register (MPR)

- ➢ **Read out predefined system timing calibration bit sequence**



- ➢ **Predefined data pattern can be loaded into MPR and read out by the external read command**
- ➢ **EMRS3 Bit A2 defines data flow from memory core or MPR. Once data flow is defined, MPR content can be continuously read by regular READ or READ with AP**

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Summary

Primary Design Challenges for a DDR3 Memory Subsystem

- **2-slot per channel DDR3 requires:**
  - **Optimization of R_{on}/ODT/C_{IO}/ZQ parameters**
- **Improved timing margins for higher performance**
  - **A leveling function for Read/Write between CLK and DQS**
  - **Tuning the signal length for CS/CLK and CTRL/Add.**

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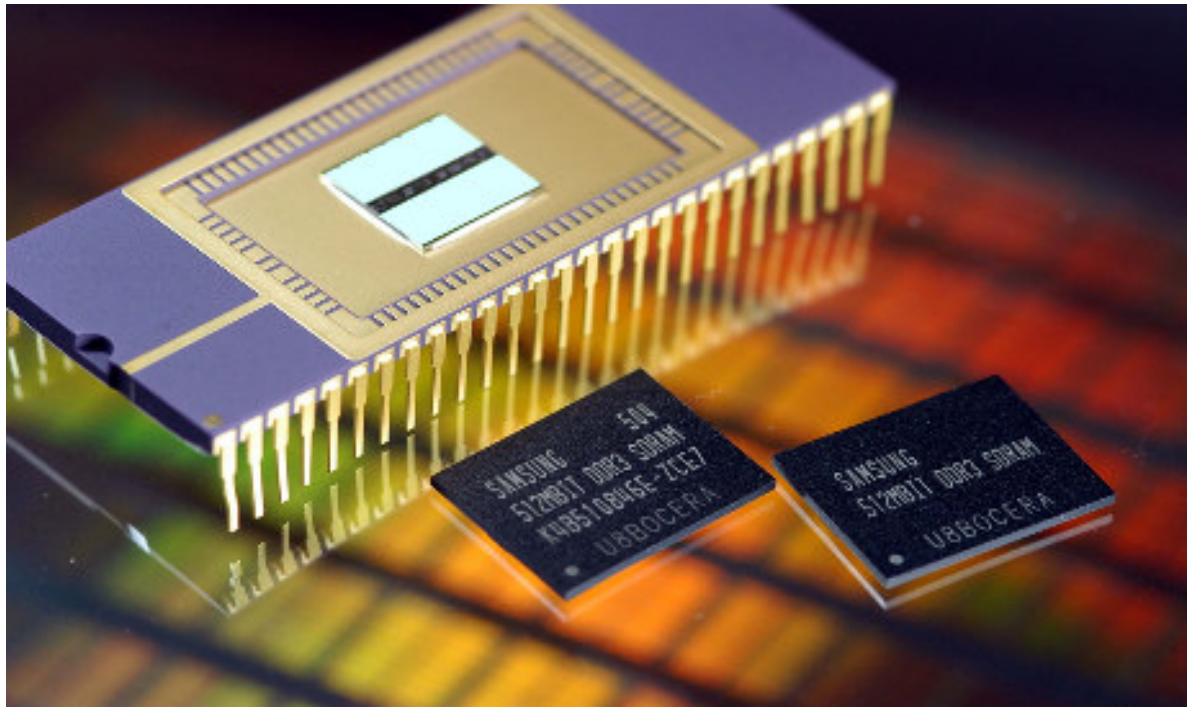
Samsung Produces World's First Working Prototype of DDR3 !!!



THANK YOU!

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